

**DISTINGUISHED LECTURE**

# Strategic Directions for Electronics Packaging



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**Abstract:** Recent advances in electronics packaging have come to the rescue as CMOS scaling has stalled making possible the incredible advances in artificial intelligence and machine learning that promise to transform our lives. This journey, however, has only just begun and much more is yet to come. The key features that will drive this transformation can be described with the simple strategy of “scale-down and scale-out” that has characterized monolithic CMOS scaling for several decades, the drive to chiplets with higher yields, and the ability to assemble a diversity of technologies on the same substrate allowing us to blur the lines between monolithic chip and a large heterogeneous assembly of chips. While we have made progress towards this goal, the technologies we have developed have ridden on legacy packaging technologies making such systems incredibly complex and expensive to build. In this talk we will describe our approach to simplify packaging at all levels: from design, architecture, process and manufacturing that have the potential to take packaging to the next level including the ability to scale packaging systematically. There are many challenges in this approach. In this talk we will outline these challenges and show that the adoption of silicon-like technology, new cooling and power delivery approaches as well as design enablement will propel packaging into the next dimension.

**Bio:** Subramanian S. Iyer (Subu) is a Distinguished Professor and holds the Charles P. Reames Endowed Chair in the Electrical Engineering Department and a joint appointment in the Materials Science and Engineering Department at UCLA. Till recently, he was on assignment to the U.S. Department of Commerce as Director of the National Advanced Packaging Manufacturing Program, where he laid the foundational strategy for the national packaging imperative. He is the founding Director of the UCLA Center for Heterogeneous Integration and Performance Scaling. Prior to that he was an IBM Fellow. His key technical contributions have been the development of the world’s first SiGe base HBT, Salicide, electrical fuses, embedded DRAM and 45nm technology node used to make the first generation of truly low power portable devices as well as the first commercial interposer and 3D integrated products. Since joining UCLA, he has been exploring new packaging paradigms and device innovations that may enable wafer-scale architectures, in-memory analog compute and medical engineering applications. He is a fellow of IEEE, APS, iMAPS and NAI as well as a Distinguished Lecturer of IEEE EDS and EPS. He is a Distinguished Alumnus of IIT Bombay and received the IEEE Daniel Noble Medal for emerging technologies in 2012 and the 2020 iMAPS Daniel C. Hughes Jr Memorial award and the iMAPS distinguished educator award in 2021.