Preliminary Exam, Fall 2013

Department of Electrical and Computer Engineering

University of California, Irvine

EECS 170B

Problem 1.

Consider the following circuit, where a saw-tooth voltage is applied at the input terminal. Draw the voltage at the output from 0 to 2T (T is the period).

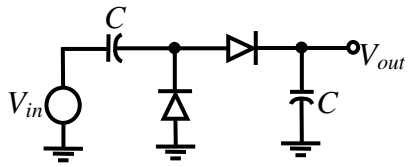
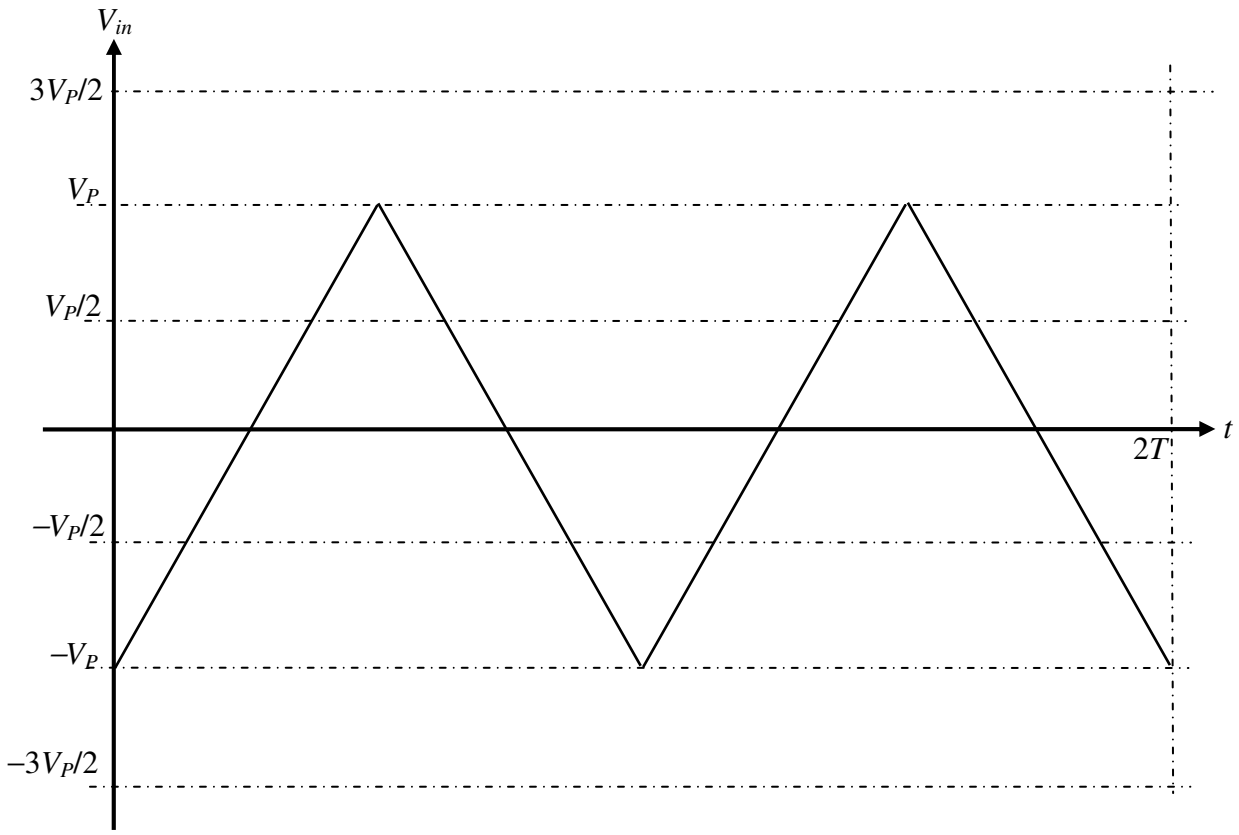


Fig. 1

– Assume that diodes are ideal with zero turn-on voltage (i.e., $V_D = 0$).

– Assume that the two capacitors in Fig. 1 are identical.

Sketch the output voltage from 0 to 2T on the same plot shown below:



Problem 2.

– Assumption 1: $V_T = kT/q = 25$ mV, $V_{BE,on} = 0.5$V, $r_b = 0\ \Omega$, $|V_A| = \infty$, $\beta_{npn} = \beta_{pnp} = 100$.

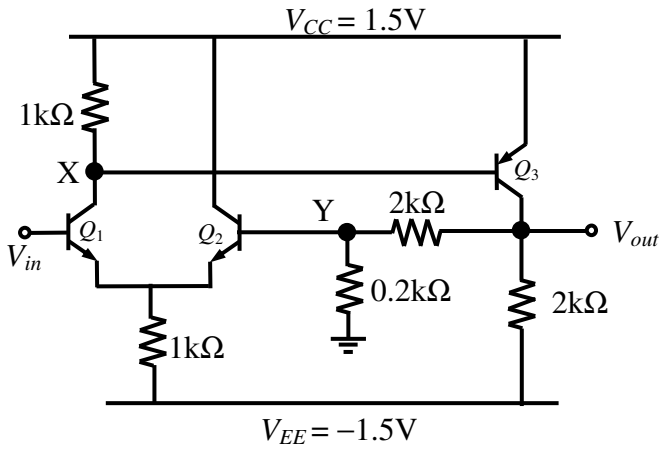
– Assumption 2: The DC input voltage $V_{in,DC} = 0$V.

Consider the following feedback amplifier, and answer the following questions:

Q1. Calculate bias DC currents of all transistors. Also, calculate the bias voltage at nodes X, Y, and output V_{out}.

Q2. Calculate the loop-gain, overall voltage gain V_{out}/V_{in}

Q3. Calculate the input and output resistance.



Problem 3.

1. Sketch CMOS realization for an XOR circuit.
2. Assume that the basic inverter has $(W/L)_N = 0.05\mu m/0.04\mu m$ and $(W/L)_P = 0.1\mu m/0.04\mu m$. Find appropriate sizes for transistors used in the XOR circuit in part 1.

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Problem 1 (20 points).

Plot the input-output characteristic of the circuit below in Fig. 1, assuming the diodes to have zero on resistance, and infinite off-resistance with $V_{D,on}$ = 0.7V.

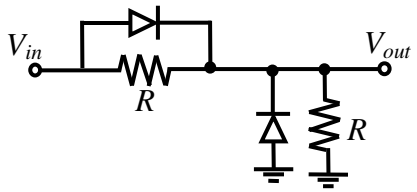

Fig. 1

Problem 2 (20 points).

Assumption: $\mu_n C_{ox} = 200\ \mu A/V^2$, $V_{THN} = 0.4V$, and ignore channel-length modulation.

1. The CMOS amplifier of Fig. 2 must be designed for a voltage gain of 5 and output impedance of 1kΩ. Bias the transistor so that it operates 100mV away from its triode region.

2. We wish to design the amplifier of Fig. 2 for maximum voltage gain but with W/L ≤ 10μm /0.04μm and maximum output impedance of 500Ω. Determine the required bias current.

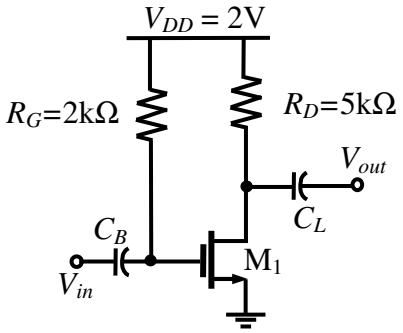

Fig. 2

Problem 3 (20 points).

Consider the following circuit (Fig. 3).

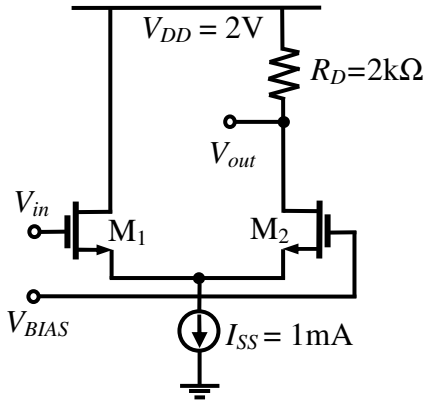

Fig. 3

The following assumptions are made:

A1. Suppose g_m = 6mA/V for all MOS transistors.

A2. Ignore the body effect and the channel-length modulation for all transistors.

Question

1. Calculate the voltage gain V_{out}/V_{in}.

Problem 4 (20 points).

Consider the following circuit (Fig. 4). Calculate I_{out} with respect to I_{REF} for the circuit of Fig. 4. Assume all transistors are operating in saturation region.

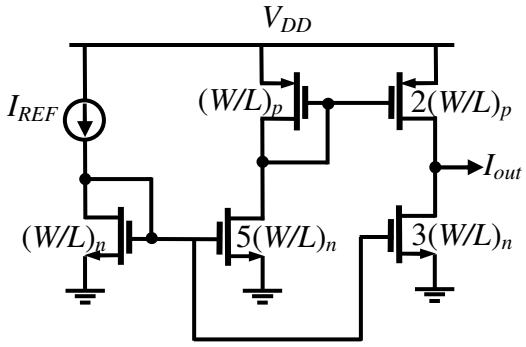

Fig. 4

Problem 5 (20 points).

What logic function the following circuit represents? (*F* is the output node)

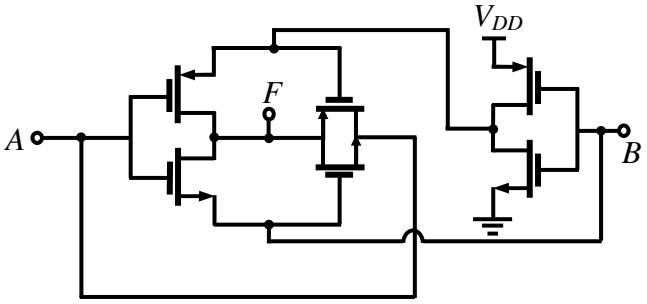

Fig. 5

Preliminary Exam, Spring 2015

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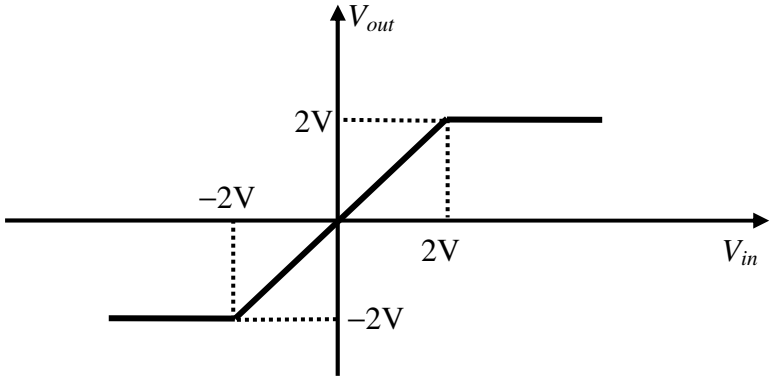
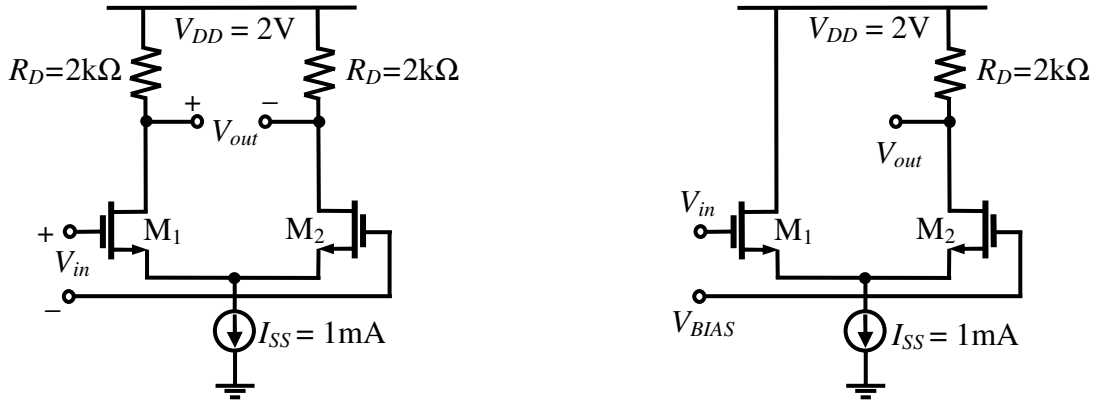
Problem 1.

Using ideal diodes ($V_{D,on}$ = 0V)and other components (i.e., batteries and resistors), construct a circuit that provides the following transfer characteristics.



Problem 2.

Consider the following two circuits.



The following assumptions are made:

A1. Suppose g_m = 6mA/V for all MOS transistors.

A2. Ignore the body effect and the channel-length modulation for all transistors.

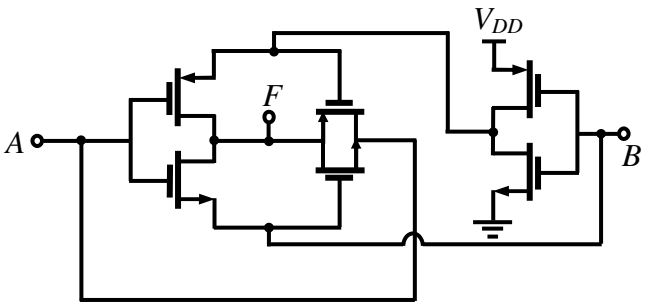
A3. The parasitic capacitances of transistors M_1 and M_2 are identical and equal to: $C_{GS,12} = C_{DB,12} = C_{SB,12} = 4C_{GD,12}$. Also, $C_{GS,12}$=50fF.

Questions

1. Compare these two circuits and describe two important differences of these circuits.
2. Calculate the voltage gain V_{out}/V_{in}.
3. Calculate 3-dB bandwidths of these two amplifiers (in MHz) using open-circuit time-constant method.

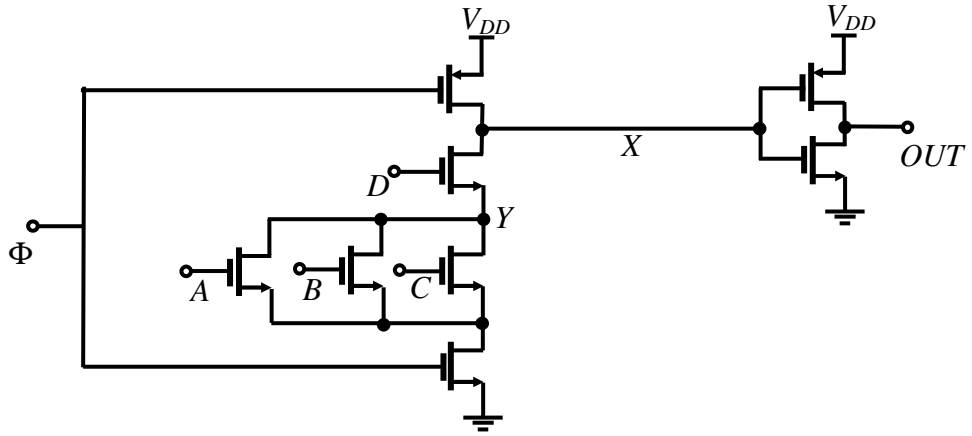
Problem 3.

What logic function the following circuit represents? (*F* is the output node)



Problem 4.

A logic gate is implemented using the following domino-logic style:



Questions:

1. What Boolean expression does the output node, *OUT*, represent in terms of A, B, C, and D?
2. Suppose that A, B, C, and D are "LOW" (logic 0) during the pre-charge. At the onset of the evaluation phase, the D input makes a 0 to 1 transition. Assuming the overall capacitance at nodes Y and X are 300fF and 100fF, respectively; what is the final value at node X with respect to V_{DD}?
3. Propose a circuit solution (by adding one transistor to the circuit) to deal with charge redistribution problem in part 2.